HIGH-SPEED SEMICONDUCTOR MEMORY HAVING INTERNAL REFRESH CONTROL

ABSTRACT OF THE DISCLOSURE

The refresh address generator of a memory includes, in part, a counter, a multitude of shift registers and multiplexers, and a comparator. With each clock cycle, the counter increments and stores the refresh count address, and the addresses stored in the counter and the shift registers prior to the increment operation is shifted out and stored in a pipelined fashion. If the array address stored in the last stage of the register pipeline is equal to the address of the array read out during the cycle immediately preceding the refresh cycle or is equal to the address of the neighboring array of the read out array, the comparator causes multiplexer to select the address stored in the counter as the refresh address. This address differs from the address of the array read out during the immediately preceding cycle by at least two counts.